What is claimed:

1. An electro-optical display device comprising:

an element substrate having:

a pixel portion including a plurality of thin film transistors;

a peripheral drive circuit portion for driving said pixel portion;

an opposite substrate being opposite to said element substrate;

a sealing member for bonding said element substrate and said opposite substrate together;

a substrate interval correction means being disposed in a sealing forming region where said sealing material is formed on the element substrate,

wherein said substrate interval correction means includes at least a conductive layer not being electrically connected to any one of the pixel portion and the peripheral drive circuit portion.

2. A device according to claim 1 wherein said substrate interval correction means includes a same material as said pixel portion.

3. A device according to claim 1 wherein said pixel portion includes a plurality of layers each being insulated by a plurality of insulating layers, and said substrate interval correction means includes a same laminate structure as said pixel portion.

4. A device according to claim 1 wherein a maximum value of a thickness of said substrate interval correction means is substantially equal to a maximum of a thickness of said pixel portion.

5. A device according to claim 1 wherein a peripheral circuit for driving said pixel portion is disposed between said pixel portion and said sealing material on said element substrate.

6. An electro-optical display device comprising:

an element substrate comprising a pixel portion having: a plurality of thin film transistors;

a plurality of signal lines and a plurality of scanning lines which are disposed in a matrix and separated from each other through a first interlayer insulation film,

a plurality of pixel electrodes being separated from the signal lines through a second interlayer insulation film, each of said pixel electrodes being electrically connected to each of the thin film transistors, and

a peripheral drive circuit portion for driving said pixel portion;

an opposite substrate being opposite to said element substrate;

a sealing material which surrounds said pixel portion and bonds said element substrate and said opposite substrate together; a substrate interval correction means being formed in a sealing forming region where said sealing material is formed on said element substrate, said substrate interval correction means comprising:

a first conductive layer comprising a same material as the scanning lines,

said first interlayer insulation film,

a second conductive layer comprising a same material as the signal lines, and

said second interlayer insulation film,

wherein said first conductive layer, said first interlayer insulation film, said second conductive layer, and said second interlayer insulation film are formed in different layers from each other.

7. A device according to claim 6 wherein said peripheral drive circuit portion for driving said pixel portion is disposed between said pixel portion and said sealing material on said element substrate.

8. A device according to claim 6 wherein an end surface of said first conductive layer of the substrate interval correction means is not superimposed on an end surface of said second conductive layer.

9. A device according to claim 6 wherein said substrate interval correction means has at least a laminate structure which is identical with a region in which said signal lines are superimposed on said scanning lines in said pixel portion.

10. A device according to claim 6 wherein a maximum value of a thickness of said substrate interval correction means is substantially equal to a maximum of a thickness of said pixel portion.

11. A device according to claim 6 further comprising:

an external circuit being formed outside the sealing forming region or an external terminal being formed outside the element substrate;

a plurality of wiring for connecting said pixel portion to said external circuit or said external terminal,

wherein each of the plurality of wiring is formed integrally with said first conductive layer, and

wherein said first conductive layer extends toward an outside of said sealing member.

12. A device according to claim 6 further comprising:

an external circuit being formed outside the sealing forming region or an external terminal being formed outside the element substrate;

a plurality of wiring for connecting said pixel portion to said external circuit or said external terminal,

wherein each of the plurality of wiring is connected to said first conductive layer inside said sealing forming region, and

wherein said first conductive layer extends toward an outside of said sealing forming region.

13. A device according to claim 6 further comprising,

an external circuit being formed outside the sealing forming region or an external terminal being formed outside the element substrate,

wherein said second conductive layer is not electrically connected to any one of said pixel portion, said external circuit and said external terminal.

14. A device according to claim 6,

wherein said first conductive layer comprises a first plurality of linear wirings being disposed at first regular intervals, and

wherein said second conductive layer comprises a second plurality of linear wirings in parallel with the signal lines or the scanning lines being disposed at second regular intervals, each of the second plurality of linear wiring being formed in a gap between the first plurality of linear wirings.

15. A device according to claim 6 wherein said first conductive layer has a zigzag shape with substantially equal width of said sealing material.

16. A device according to claim 6 wherein said first conductive layer is substantially equal to a pitch of said pixel electrode.

17. A device according to claim 6,

wherein said pixel portion further includes a plurality of thin-film transistors for driving said pixel electrodes,

wherein said first conductive layer is formed together with said scanning lines, and said second conductive layer is formed together with said signal lines.

18. An electro-optical display device comprising:

an element substrate comprising a pixel portion having:

a plurality of signal lines and a plurality of scanning lines which are disposed in a matrix and separated from each other through a first interlayer insulation film,

a plurality of pixel electrodes disposed on cross points of said signal lines and said scanning lines and separated from the signal lines through a second interlayer insulation film,

a plurality of thin film transistors each for operating each of the pixel electrodes, and

a peripheral drive circuit portion for driving said pixel portion;

an opposite substrate being opposite to said element substrate;

a sealing material which surrounds said pixel portion and bonds said element substrate and said opposite substrate together;

a substrate interval correction means being formed in a sealing forming region where said sealing material is formed on said element substrate, said substrate interval correction means having:

at least a conductive layer comprising a same material as the scanning lines,

said first interlayer insulation film, and

said second interlayer insulation film,

wherein said conductive layer, said first interlayer insulation film, and said second insulation film are formed in different layers from each other,

wherein said conductive layer is not electrically connected to any one of the pixel portion and the peripheral drive circuit portion.

19. A device according to claim 18 wherein said peripheral drive circuit portion for driving said pixel portion is disposed between said pixel portion and said sealing material on said element substrate.

20. A device according to claim 18 further comprising:

an external circuit being formed outside the sealing forming region or an external terminal being formed outside the element substrate;

a plurality of wiring for connecting said pixel portion to said external circuit or said external terminal,

wherein each of the plurality of wiring is formed integrally with said conductive layer, and

wherein said conductive layer extends toward an outside of said sealing member.

21. A device according to claim 18 further comprising:

an external circuit being formed outside the sealing forming region or an external terminal being formed outside the element substrate;

a plurality of wiring for connecting said pixel portion to said external circuit or said external terminal,

wherein each of the plurality of wiring is connected to said conductive layer inside said sealing forming region, and

wherein said conductive layer extends toward an outside of said sealing forming region.

22. A device according to claim 18 wherein said conductive layer is disposed along an edge portion of said element substrate and has a plurality of branches.

23. A device according to claim 22 wherein the branches of said conductive layer are formed in an outer portion of said sealing forming region.

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